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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,653	03/16/2004	Chau-chin Su	06720.0122-00	1121
22852 7590 11/14/2007 FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			EXAMINER FOTAKIS, ARISTOCRATIS	
			ART UNIT 2611	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/800,653

Applicant(s)

SU ET AL.

Examiner

Aristocratis Fotakis

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09/28/2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 – 3, 5 – 7, 11 – 13 and 16 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,850,422) in view of Lee et al. ("*An 84-mW 4-Gb/s Clock and Data Recovery Circuit for Serial Link Applications*", VLSI Circuits Symposium, Kyoto, Japan, June 2001).

Re claims 1 and 11, Chen teaches of a method and a system comprising: a clock for generating a clock signal from a signal source(#12, Fig.1 and Fig.2, Col 3 Lines 59 – 67); a phase detector coupled to the clock and the signal source for oversampling the transmitted serial data and providing sampled data (#14, Fig.1, Col 4, Lines 35 – 45) and for detecting and grouping phase transitions between a phase lead and a phase lag (#18, Fig.1) in the sampled data and outputting phase transition data (#50, Fig.6A); a phase selector (#16, CLOCK MUX, Fig.1); an encoder (#52, combinational logic, Fig.6A), coupled to the phase detector (Fig.1 and 6A), for encoding the phase transition data (#52, combinational logic, Fig.6A, truth table, Fig.6B) according to an optimum phase selected by the phase selector (#48, Fig.1 and Fig.6A); and; a confidence counter (#20, Fig.1) coupled to the encoder (#52, Fig.6A) to receive the encoded phase transition data (output from encoding in #18) and provide an output representative of an accumulated effect (Col 1, line 67 to Col 2, Lines 1 – 5) of the phase transitions based on the encoded phase transition data (Col 6, Lines 36 – 67 and Col 7, Lines 1 - 19);

wherein the phase selector (#16, CLOCK MUX, Fig.1) is coupled to receive the clock signal and the output from the confidence counter (#20), to select an optimum phase effective for recovering the clock relative to the transmitted serial data (Fig.4, Col 4, Lines 66 – 67 to Col 5, Lines 1 – 19 and Fig.1). However, Chen does not teach of a clock signal generated in half the rate of the transmitted serial data signal.

Lee teaches of a 4Gb/s serial link tracking clock and data recovery (CDR) circuit fabricated in 0.24mm CMOS technology dissipates 84mW and occupies 0.3mm². The input signal is 2xoversampled by 8 offset-cancelled receive amplifiers per receive clock cycle. The samples are processed by a phase controller to position the receive clocks at the center and the edge of the data eye using a semi-digital dual delay-locked loop (DLL) (Abstract). The 8 phases generated are used to perform 2xoversampling on the incoming data. The bit rate is 4x the receive clock rate. Before feeding into the phase controller, the resulting data samples are further demultiplexed to half the receive clock rate to relax the frequency requirement of the digital logic (System Architecture, Page 1). However, Lee does not specifically teach of an exactly half clock rate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used fractional clock rate that would for an effective small, low-power, and noise insensitive high speed serial link design (Conclusion, Page 3).

It would have been an obvious matter of design choice to generate the clock signal in half the rate of the transmitted serial data signal. Applicant has not disclosed that a clock signal generated in half the rate of the transmitted serial data signal

provides an advantage over a clock signal generated in a fractional rate. One of ordinary skill in the art would have used a fractional clock rate such as half rate to reduce power consumption.

Re claims 2 – 3 and 12 - 13, Chen teaches of the phase detector oversampling the transmitted serial data at ten times the rate of the transmitted serial data wherein the clock signal has ten phases for each period in the transmitted serial data.

Chen does not disclose of oversampling the transmitted data at four times the sampling rate wherein the clock signal has eight phases for each period in the transmitted serial data. It would have been an obvious matter of design choice to oversample the transmitted serial data at four times the rate of the transmitted serial data wherein the clock signal has ten phases for each period in the transmitted serial data. Applicant has not disclosed that the 4Xoversampling rate wherein the clock signal has eight phases for each period in the transmitted serial data provides an advantage or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicants invention to perform equally well with providing the ten phase used for oversampling rate for better noise or jitter tolerance (Col 4, Lines 35 – 38).

Re claim 5, Chen teaches of the clock comprising a phase locked loop (#12, PLL, Fig.1 and Fig.2).

Re claim 6, Chen teaches of the confidence counter comprising a state machine (#20, Fig.1 and Fig.7) for identifying each of the detected phase leads and the detected phase lags (output from #18, Fig.1).

Re claims 7 and 17 - 18, Chen teaches of the state machine further comprises an initial state (move around *ideal position*, Col 6, Lines 45 - 51), ten states for each detection of the phase lead, and ten states for each detection of the phase lag (shifting left or right, Col 6, Lines 45 - 55). The number of states is the number of phases used. The number of phases was a designer's choice as discussed above.

Re claim 16, Chen teaches of a system comprising: a clock for generating an 8-phase clock signal at half rate of transmitted serial data (see claim 3); a half-rate phase detector for oversampling the transmitted serial data at four times the half clock rate and providing sampled data, and for detecting phase transitions between a phase lead and a phase lag in the sampled data and outputting phase transition data; a phase selector; an encoder encoding the phase transition data according to an optimum phase selected by the phase selector; and a confidence counter coupled to receive the phase transition data and provide an output representative of an accumulated effect of the phase transitions; wherein the phase selector is coupled to receive the clock signal and the

output from the confidence counter, to select an optimum phase effective for recovering the clock relative to the transmitted serial data (see claim 1).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Nakamura (US Pub 2002/0030522).

Chen teaches all the limitations of claim 1 except of the use of the clock comprising a DLL.

Nakamura teaches of an oversampling clock recovery circuit (title of invention) where a relatively small number of clocks are supplied, and controlled in phase by a phase control circuit. From the phase-controlled clocks, a delay-locked loop (DLL) generates a relatively large number of clocks (multiphase clocks) required for phase comparison, and supplies generated clocks to the phase comparators for phase comparison (Paragraph 0028).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a DLL to generate a relatively large number of clocks (multiphase clocks) required for phase comparison, and supply generated clocks to the phase comparators for phase comparison.

Claims 8 – 9, 15, 19 and 23 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chen in view of Huang et al.(US 7,113,560).

Re claims 8 and 19, Chen teaches all the limitations of claims 1 and 16, except of a state machine having four states for shifting the sampling phase toward the optimum phase.

Huang teaches of a method and circuit to produce an optimal sampling phase for recovery of a digital signal. A digital signal is *over-sampled* by sampling on each phase of a *multiple phase clock* to generate a sample value per phase. The multiple phase clock may be generated by a *DLL*. A voted value is determined per phase comprising a majority value of a set of consecutive sample values. *Transition phases* are sensed. A transition phase is defined as two consecutive voted phases comprising different values. The transition phases are compared to a stored phase state to determine a *signal shift direction*. The signal shift direction is filtered to generate a state update signal. The stored phase state is updated based on the state update signal. The stored phase state corresponds to an optimal sampling phase for recovery of the digital signal (Abstract, Figs.2, 4, 6, 7, 10). The phase selector (#56, #60, Fig.2, Fig.4) comprises a state machine (#126, Fig.6) having five states for shifting the sampling phase toward the optimum phase (Fig.7, Col 6, Lines 58 – 67 to Col 7, Lines 1 - 6).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a state machine to shift the phase state corresponding to the optimal phase for recovery of the digital data. (Col 6, Lines 64 – 67). As discussed

earlier, it would have been an obvious matter of design choice to select the number of states of interest.

Re claims 9 and 15, Chen teaches all the limitations of claims 1 and 11, except of the phase detector performing XOR logic operations.

Huang, teaches of the transition phase sensor (#106, Fig.4) as an XOR function (#114, Fig.5). The XOR function detects a 0,1 or a 1,0 sequence in the voted data $V(n-1:n)$. The transition value T_n is set when a transition is detected.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used an XOR logic function for its high speed operation to detect a 0,1 or a 1,0 sequence and set the transition value T_n when a transition is detected.

Re claim 23, Chen teaches of encoding the output data of the phase detector according to the optimum phase of the phase selector (recovered clock from #16, Fig.1).

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Huang as applied to claim 9 in view of Kim et al. ("*Clock and data recovery circuit with two exclusive-OR phase frequency detector*", Electronic Letters, Vol.36, No.16, 1347–1349, 3rd August 2000).

Chen and Huang teach all the limitations of claim 9 except of specifically teaching of the XOR logic gate having a phase transition rate twice of phase resolution of the phase detector and the XOR logic operation results are grouped into two sets according to sampled clock phases.

Kim teaches of a simple phase-locked loop with a PFD of two-XOR logic gates and a data retiming block. The loop components in the PLL, such as the two-XOR PFD, charge-pump, loop filter and VCO, combine to cancel the phase and frequency error between the input data and recovered clock. The first XOR gate in the PFD is used to produce the data-lead signal and the second XOR gate produces the data-lag signal. The VCO composed of four differential buffer stages generates eight differential clocks each spaced by 45°. The recovered clock used for data retiming comes from the first delay stage of the VCO. Double-edge triggered D-FF is used to produce the retimed data. By using the double-edge triggered D-FF, the clock rate can be reduced to one half of the data rate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used Kim's two sets of XOR logic gates having a phase transition rate twice of phase resolution of the phase detector by using the double-edge triggered D-FF to build an effective high speed CMOS CDR circuit having a simple structure and that can be realized in a small area and being able to cancel the phase and frequency error between the input data and recovered clock.

Claims 10, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Maddux (US Pub 2003/0061564).

Chen teaches all the limitations of claim 1, 11 and 16 except of a multiplexer coupled to receive the recovered clock and the oversampled data and output the transmitted data.

Maddux, teaches of a data recovery system which comprises of a selector (#208, Fig.2, multiplexer) coupled to receive the recovered clock (from #206) and the oversampled data (from #202) and output the transmitted data (recovered data).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a selector to reliably pass the sample which the decision matrix selects.

Response to Arguments

Applicant's arguments filed September 28, 2007 have been fully considered but they are not persuasive.

Applicants have submitted that Chen is completely silent on "an encoder", coupled to the half-rate phase detector, for encoding the phase transition data according to an optimum phase of the phase selector.

As discussed above, the Examiner has submitted that the combinational logic #52 (Fig.6A) performs the operation of an encoder by the use of a truth table (Fig.6B) similar to Applicants encoder as described in Paragraphs 0045 – 0046 and Table 3 of Applicants specification.

Applicants have submitted that Chen does not teach of a half-rate 4xoversampling phase detector. The Examiner has presented the reference of Lee et al (please see above) where Lee teaches of a fractional clock rate and oversampling. Eventhough, Lee and Chen do not disclose the same values for the clock rate, oversampling and the number of clock phases used; it would be a matter of design's choice to use Applicants values, since the objective of Lee's publication and Chen invention is to reduce power consumption.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF


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SUPERVISORY PATENT EXAMINER